Digital PSU
Plant Measurement

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Biricha Digital Workshops

- The following are just some slides from our workshops.
- Why not attend one our Analog or Digital PSU design workshops?
- We run them regularly in Germany and the US...

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Digital Power & Digital PFC Workshop

- **Day 1: Introduction to Digital Power**
  - Introduction to digital power, setting up digital power peripherals (PWMs, ADCs, etc.), number representation on MCUs
  - Day 1 Lab exercises
- **Day 2: Digital Voltage Mode Control**
  - Analog transfer function H(s), phase margin, gain margin and stability, analog compensator design, digital transfer functions, discrete time z & bi-linear transforms, digital compensator design
  - Day 2 Lab exercise
- **Day 3: Digital Current Mode Control**
  - Digital peak current mode control, peak current mode model and compensator design slope compensation, sub-harmonic oscillations and stability
  - Day 3 Lab exercises
- **Day 4: Digital PFC**
  - Step-by-step digital PFC control theory and operation, digital voltage loop current loop and voltage feed forward design, digital PFC software structure, linear difference equations and correct scaling, digital PFC implementation
  - Day 4 Lab exercises

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Analog Power & Analog PFC Workshop

- **Day 1: Introduction to PSU Design and Voltage Mode Control**
  - Topology selection guide, transfer functions and frequency domain design, Bode plots, poles and zeros, capacitor ESR, stability criteria, analog compensators, voltage mode control, Frequency response design
  - Day 1 Lab exercises
- **Day 2: Peak Current Mode Control**
  - Peak current mode control, sub-harmonic oscillations, slope compensation, right hand plane zeros, Flyback PCMC controller, Transformer selection, non-isolated bias supplies, output filter design, snubber design
  - Day 2 Lab exercise
- **Day 3: Isolated PSU and Bias Supply Design**
  - Isolated power supply design, isolated compensator design with TL431/LMV431, opto characteristics, programmable reference stability, real life design examples, isolated flyback design
  - Day 3 Lab exercises
- **Day 4: Analog PFC**
  - Fundamentals of power delivery, step-by-step Analog PFC control theory, analog voltage loop, current loop and voltage feed forward design, PFC design and implementation
  - Day 4 Lab exercises

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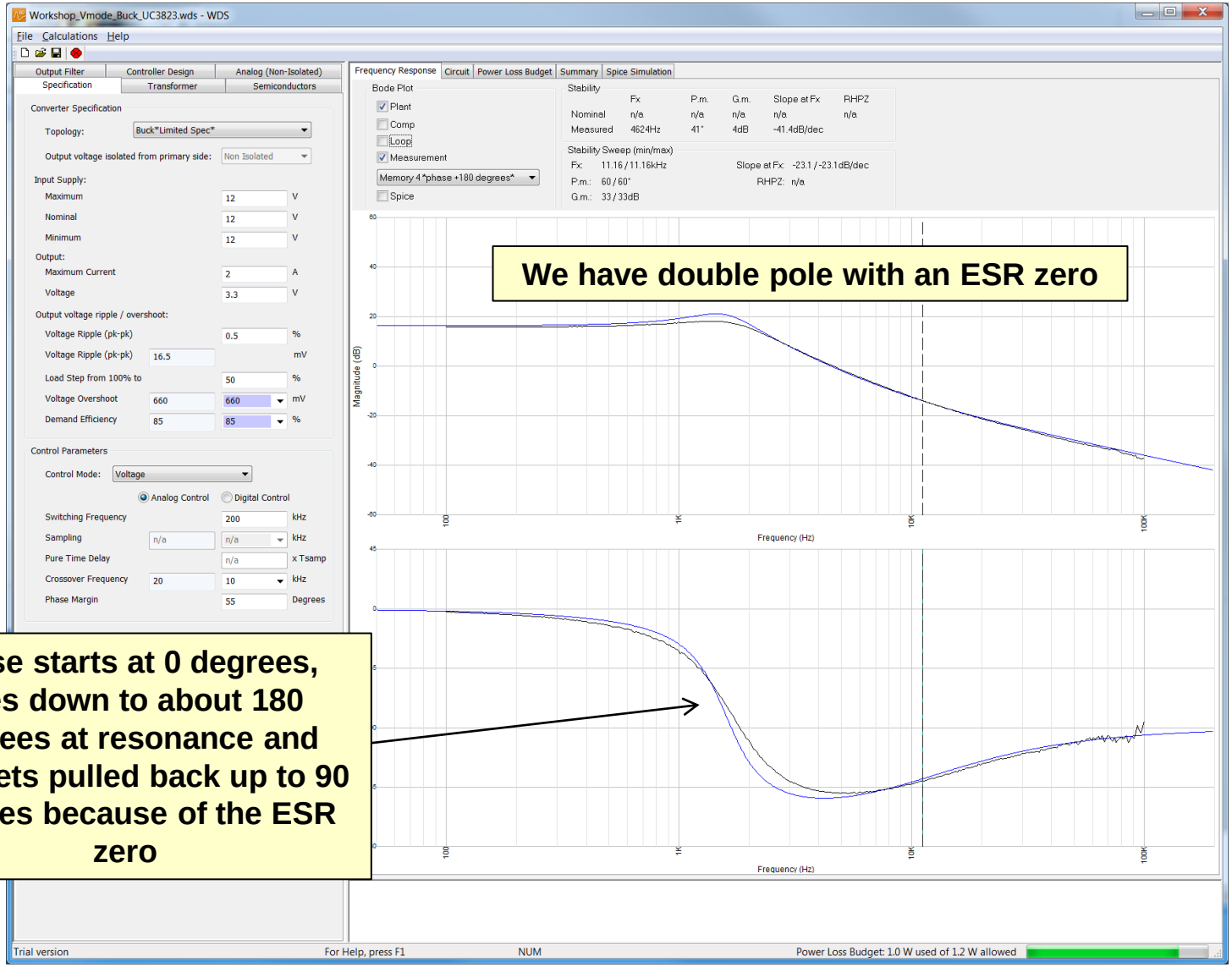
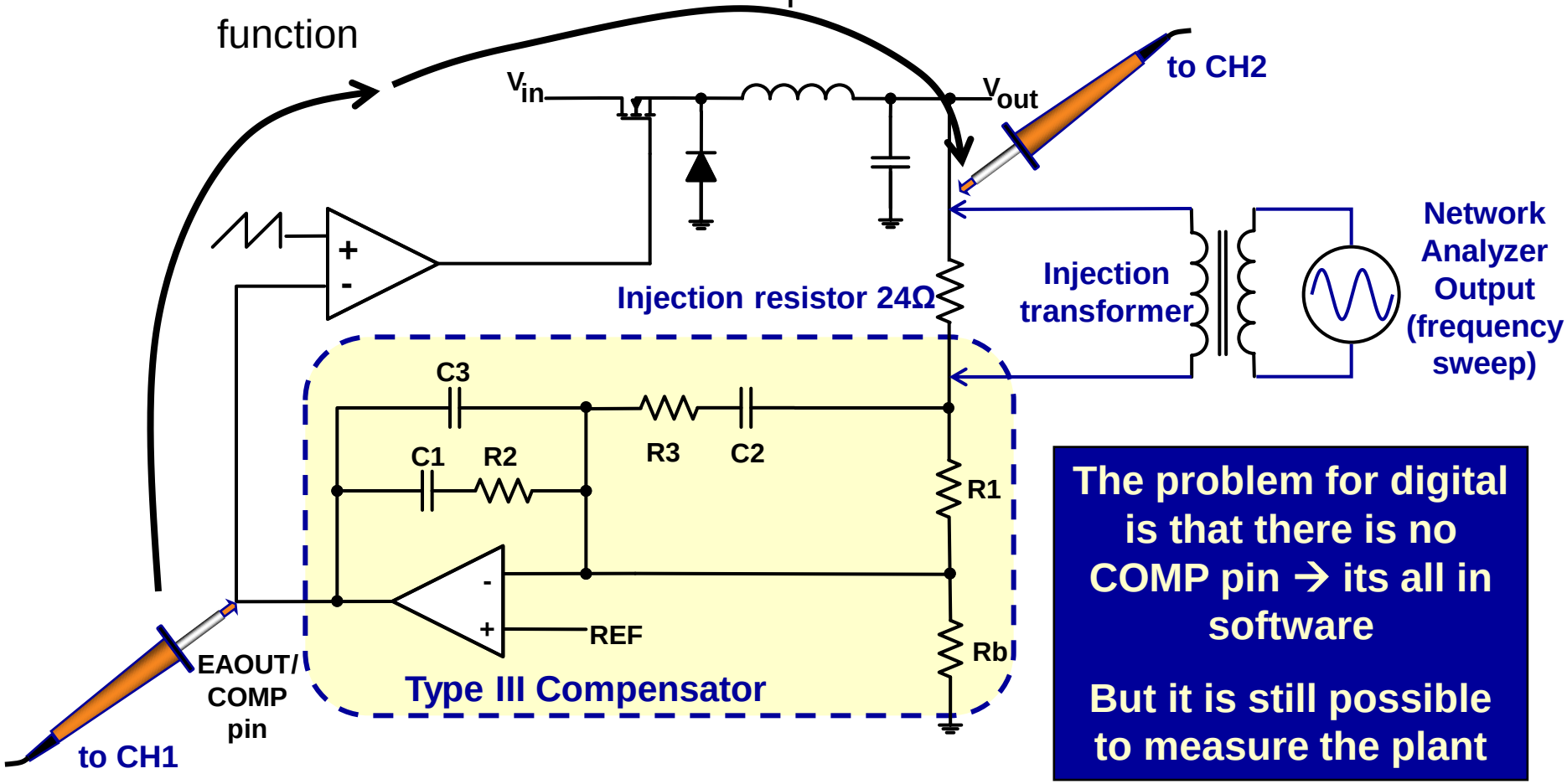
Plant of a CCM Voltage mode Buck Converter typically looks like this:



Phase starts at 0 degrees, goes down to about 180 degrees at resonance and then gets pulled back up to 90 degrees because of the ESR zero

Analog Plant Measurement

- Measure the plant:
  - Also known as the control to output transfer function



The problem for digital is that there is no COMP pin → its all in software

But it is still possible to measure the plant

Measuring Plant of the Digital PSU

- Our problem is that we can only measure the “loop”
- The power supply has some scaling factors
  - Gain of the ADC potential divider
  - Gain of the ADC itself
  - Gain of the PWM block
- For simplicity let us assume that the gain of all of the above is 100
  - So we have our plant scaled by 100
- If we now add a simple proportional compensator with a gain of 0dB (i.e. Kp = 1) and measure the “loop” we will in fact see the plant
  - Because the compensator gain Kp is 0db it has no impact on the bode plot
  - But our measurement will be off by a factor of 100
  - So all we have to do is to set Kp to 1/100, then measure the loop and we will in fact see the plant
  - We must still adjust the phase of the plant but we will talk about that shortly

How to Calculate Kp so that the Overall Gain = 0dB

- We need to set our Kp so that the overall gains are negated; for voltage mode set Kp to:

$$Kp = \left(\frac{1}{ADC\ Pot\ Scale\ Factor} \right) \times \left(\frac{ADC\ Range\ in\ Volts}{\left(2^{ADC\ bits} - 1\right)} \right) \times \left(PWM\ Period\ in\ Ticks \right)$$

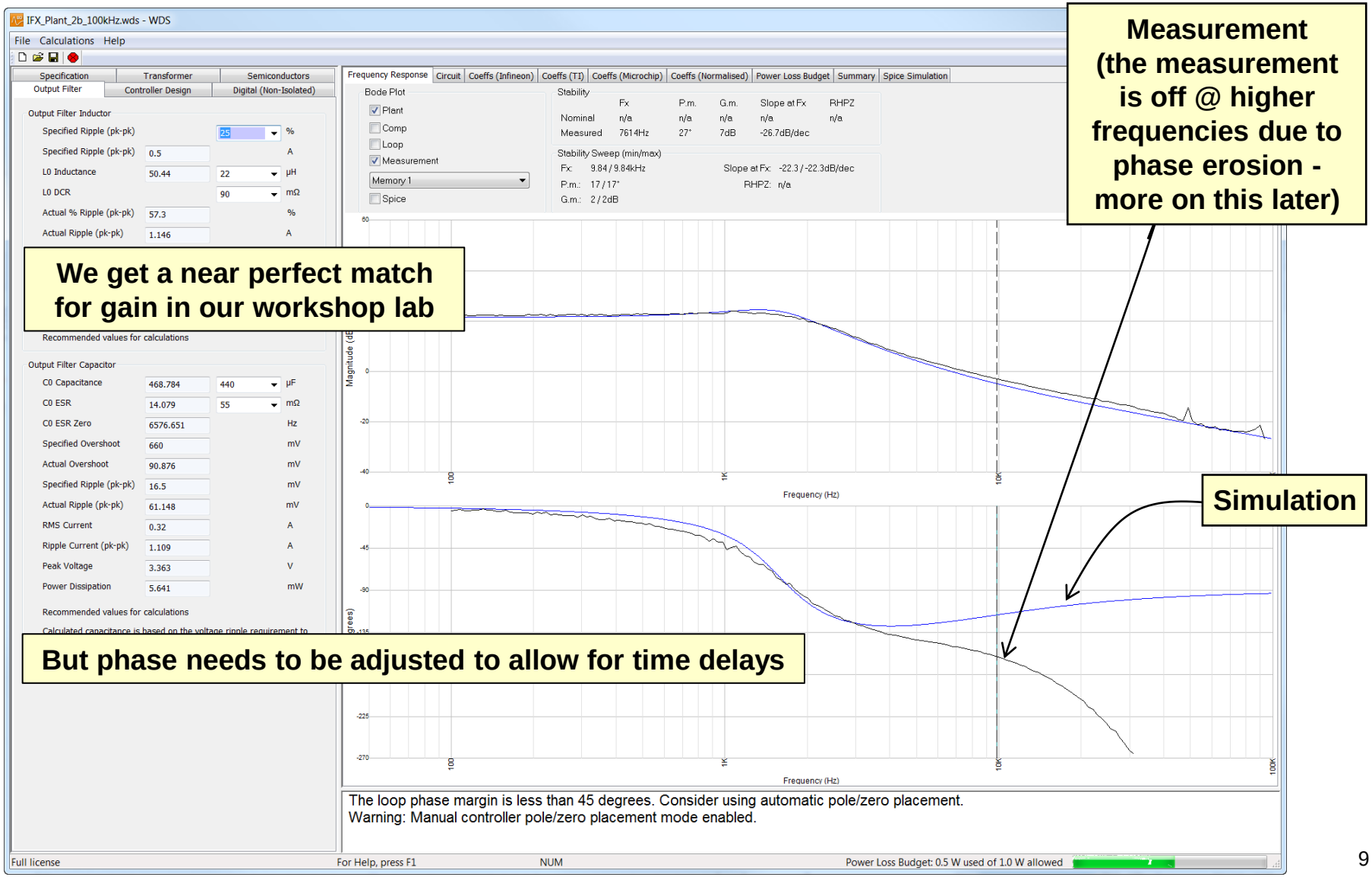
- Design Example:
  - 200 kHz PWM with 12 bit ADC and a 4.096 GHz Hi-Res PWM clock and a potential divider with a Gain of 0.785
  - Period = 20480 ticks & ADC quantization levels = 4095

$$Kp = \left(\frac{1}{0.785} \right) \times \left(\frac{3.3}{4095} \right) \times \left(20480 \right) = 21.02$$

Note: Analog power supply should be designed with a normalized PWM ramp i.e. 0→1V

BIRICHA DIGITAL

Real & Simulated Plant for One of Our Lab Power Stages



Measurement (the measurement is off @ higher frequencies due to phase erosion - more on this later)

We get a near perfect match for gain in our workshop lab

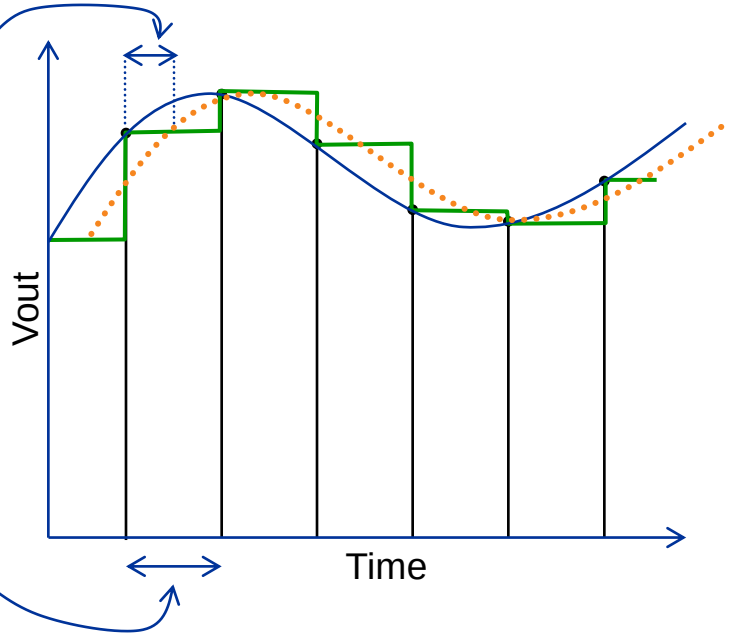
Simulation

But phase needs to be adjusted to allow for time delays

Phase Erosion in Digital World

- Because our plant measurement is still going through sample and reconstruction, there will be some phase loss → but in the case of the plant this is not real it is only an artifact of the way that we are measuring.
- There are two mechanisms that introduce phase lag in to our digital power supply:
  - The sampling and reconstruction process AND the time taken from the time we sampled our voltage to the time we carried out our calculations i.e. Time delay, Td
  - The earlier we take our sample, the more the time delay and hence the phase loss
  - Typically we sample at the beginning of the cycle so we have 1 Ts worth of pure time delay

Reconstructed signal after the DAC (i.e. PWM). This has a time delay of 0.5Ts.



Sampling interval Ts = (1/ Fs)

All we need to do to correct our plants phase plot is to add the extra phase loss that we are erroneously measuring

Luckily this is very simple

Phase Erosion in Digital World

- For a pure sine wave, phase delay ϕ at a certain frequency f is given by:

$$\phi = 360° \times f \times Time\ Delay$$

  - The sampling process and reconstruction introduces a time delay of 0.5xTs. Therefore the phase margin erosion at 10kHz with a switching frequency of 200kHz would be:

$$\phi_{sampling} = 360° \times f \times \frac{T_s}{2}$$

(360º x 10kHz x 5µs /2) = 9º

  - Phase margin erosion at 10kHz due to calculation delay:

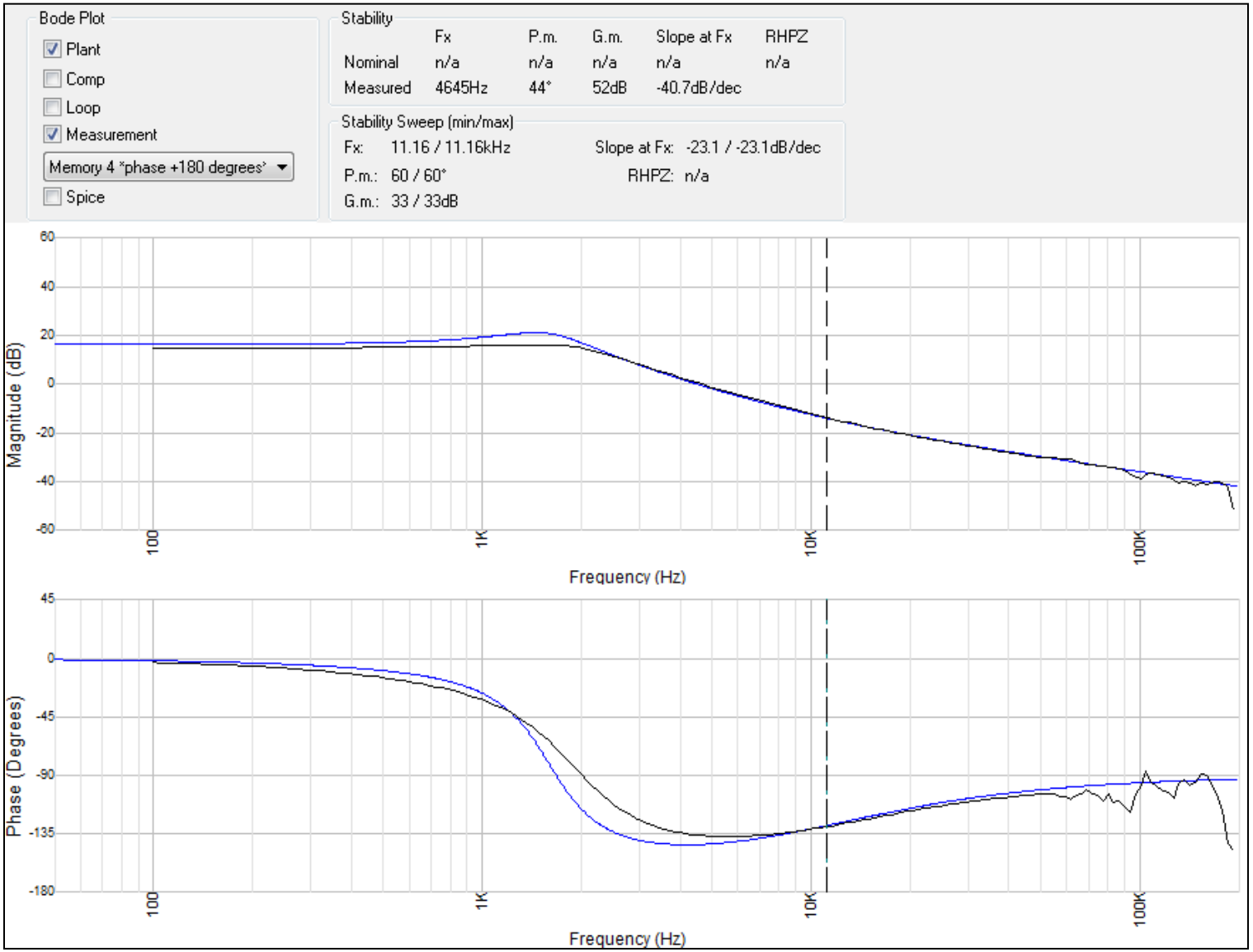
$$\phi_{calculation} = 360° \times f \times k\,T_s$$

(360º x 10kHz x 5µs x 1 = 18º

Where:
k = in the number of sampling intervals (need not be an integer).
Worst case scenario: we do the calculation at the beginning of the first sampling interval and update in the next; therefore k = 1

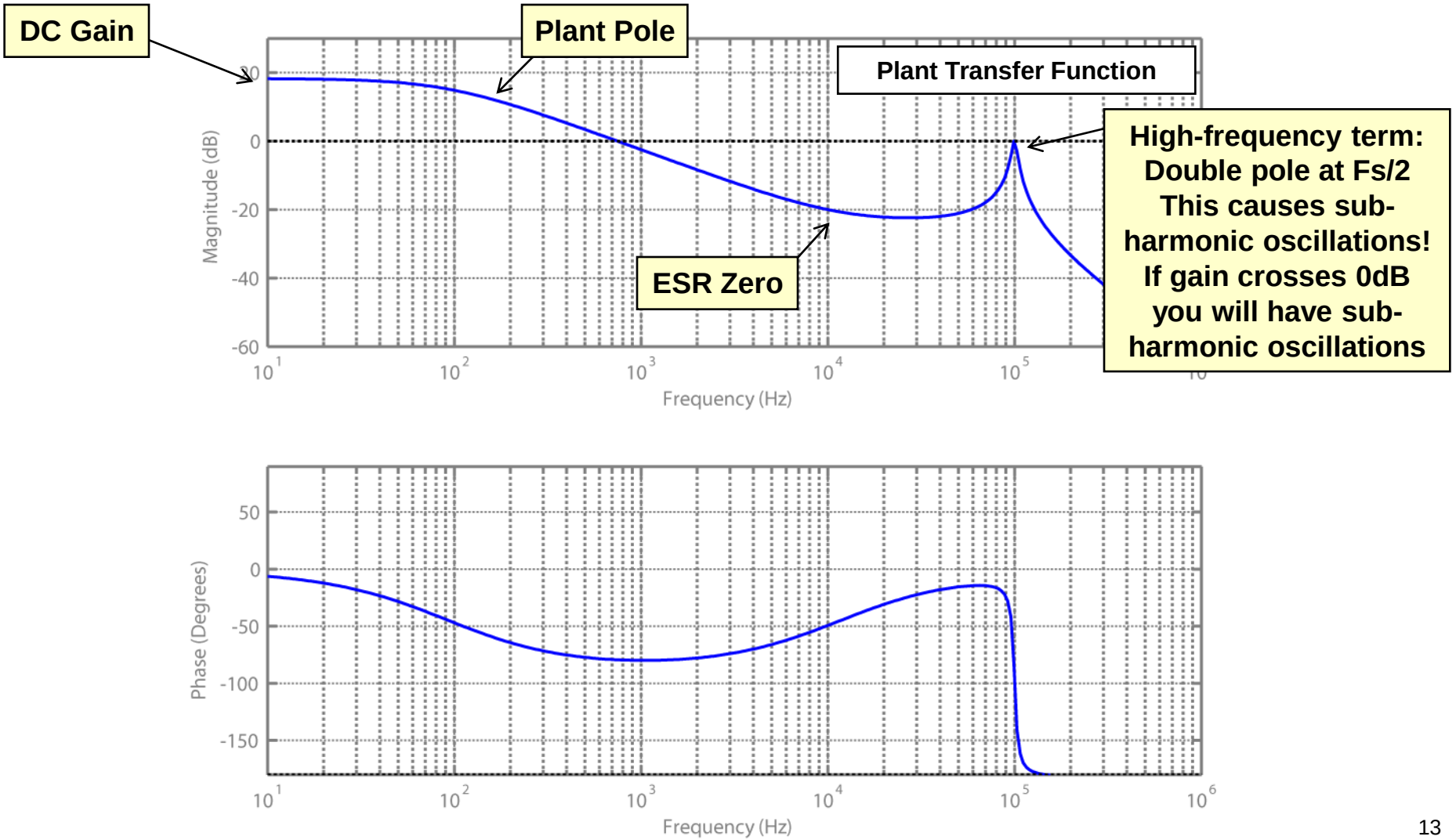
You can see that the measurement error in our phase can be "exactly" calculated from the above 2 equations and corrected on the plot

Real life Plant with Phase Corrected



Peak Current Mode Plant

- The Bode plot of the peak current mode transfer function will look similar to this:



Calculating the Scaling Factor Kp

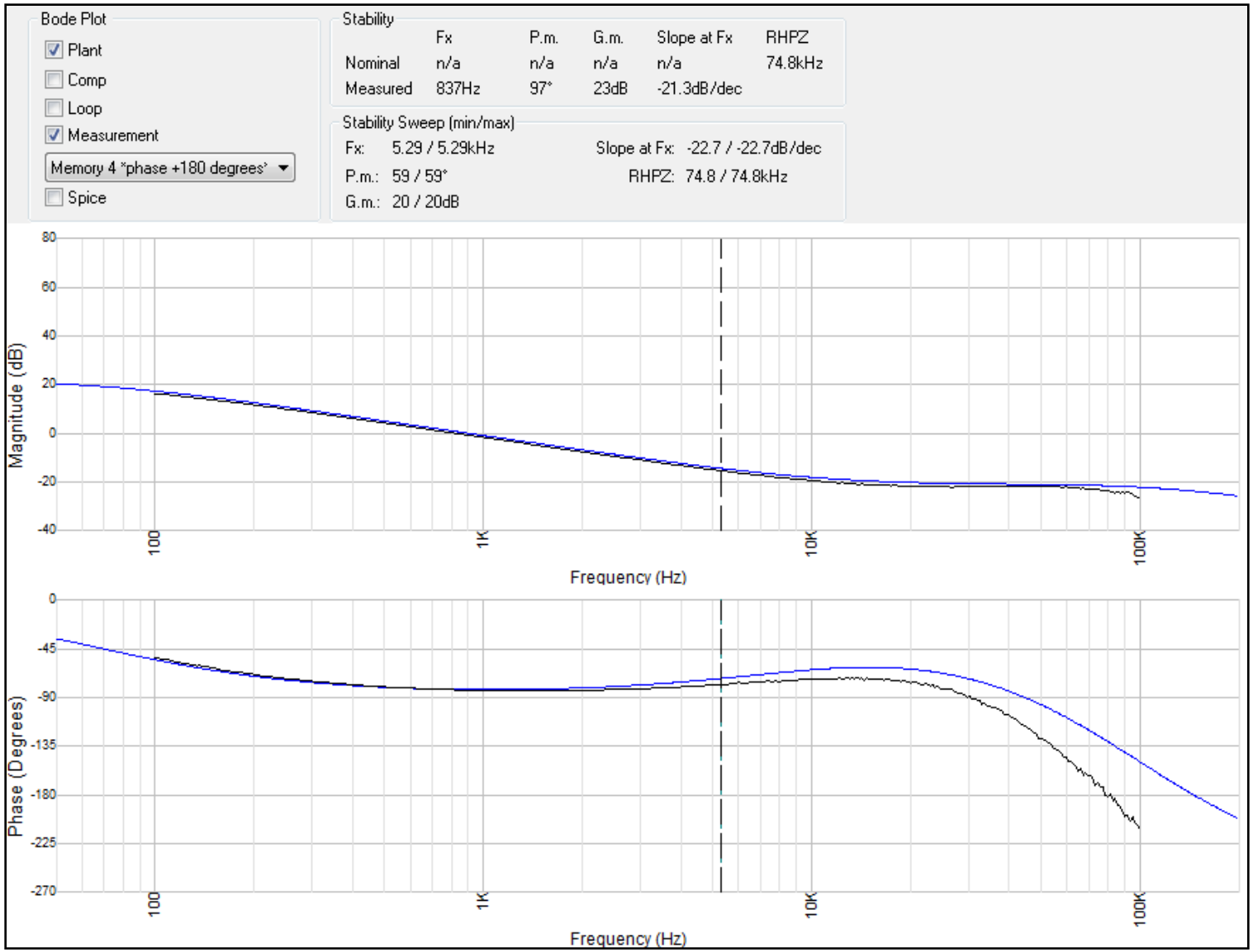
- The procedure is exactly the same as voltage mode
- We have exactly the same gains as voltage mode but now we also need to take into consideration the scaling effects of the DAC

$$Kp = \left(\frac{1}{ADC\ Pot\ Scale\ Factor} \right) \times \left(\frac{ADC\ Range\ in\ Volts}{\left(2^{ADC\ bits} - 1\right)} \right) \times \frac{\left(2^{DAC\ bits} - 1\right)}{DAC\ Range\ in\ Volts}$$

In the case of our Buck converter running an MCU with a 12 bit ADC and a 12 bit DAC:

Kp = (1 / 0.785) x (3.3 / 4095) x (4095 / 3.3) = 1.27

Real life Plant with Phase Corrected



Taken from Biricha's Digital Power Workshop

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