Foundations (Part 2.B) - Voltage Mode PSU Compensator Design

tags: voltage mode control, poles and zeros

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Introduction

In the previous article we discussed power supply compensators in detail; we can now design our first compensator to stabilise a voltage mode, Forward type power stage. The design method presented here can be applied to all hard-switched "non-isolated" Forward type converterswith or without atransformer (i.e.Buck, Forward, Push-Pull, Half-Bridge, Full Bridge). We will discuss current mode control and opto-isolated power supply design in great detail in future articles.

But first let us have a quick word about voltage mode control. Voltage mode is one of the earliest forms of switch mode power supply control and its operation is very simple.

All we have to do is to look at the output voltage; if it goes up with respect to the desired value, we reduce the PWM duty and if it goes down we increase it. As such, all we are doing is regulating the output voltage with respect to our desired "reference" voltage.

Of course the manner with which we change this duty is dictated by the compensator that we design i.e. the position of its poles and zeros. The compensator should give us good transient performance, whilst at the same time make sure that we do not violate the stability criteria.

Voltage Mode Compensator Design

For voltage mode control we almost always need a Type III compensator. The circuit for our Type III compensators is given in Figure 1.
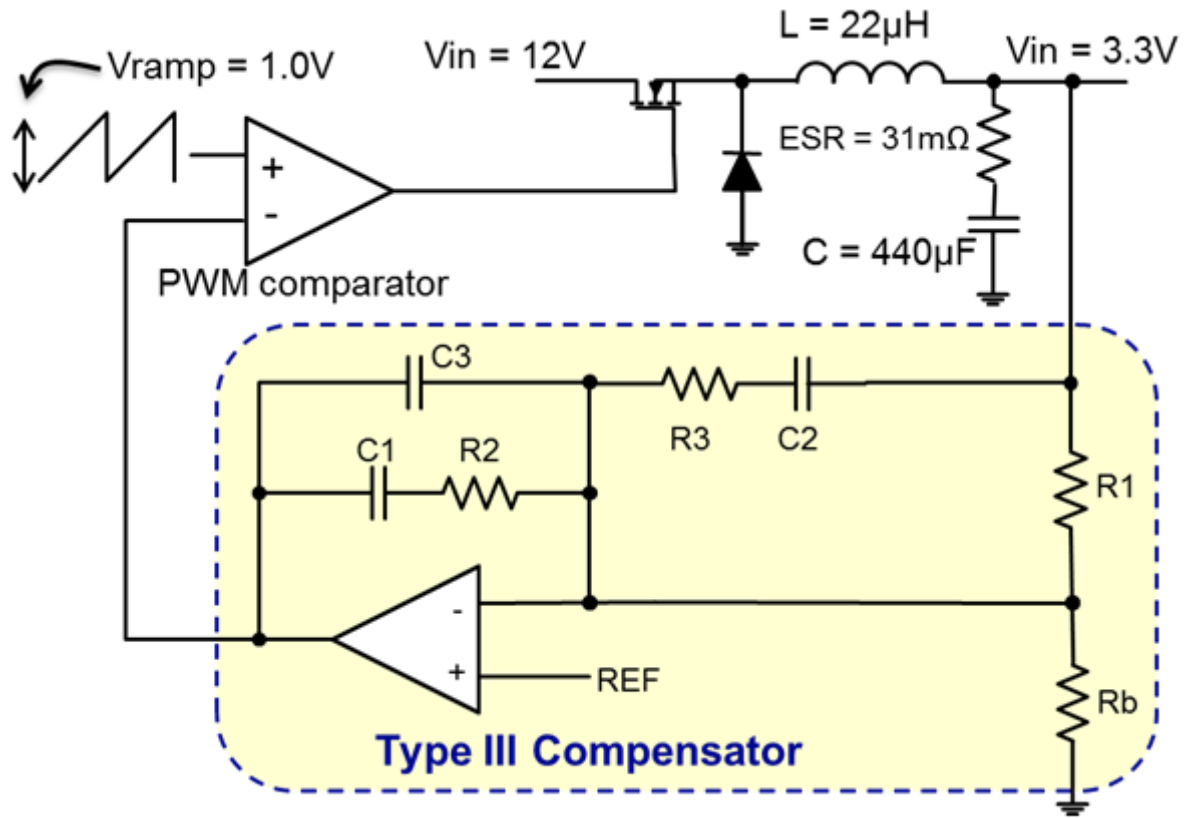
Figure 1. Type III compensator.

From previous articles we know the transfer function, Hc(s), and equations relating the poles and zeros to component values:

$$H\left(s\right) = \left(\frac{\omega_{p0}}{s}\right) \frac{\left(\frac{s}{\omega_{z1}} + 1\right)\left(\frac{s}{\omega_{z2}} + 1\right)}{\left(\frac{s}{\omega_{p2}} + 1\right)\left(\frac{s}{\omega_{p3}} + 1\right)}$$

Equation 1

Please note that these are in radians per second but we usually work in Hz so please don't forget that 2π scaling factor.

$$\omega_{p0} = \frac{1}{R_1\left(C_1 + C_3\right)}$$

$$\omega_{p2} = \frac{\left(C_1 + C_3\right)}{R_2 C_1 C_3}$$

$$\omega_{p3} = \frac{1}{R_3 C_2}$$

$$\omega_{z1} = \frac{1}{R_2 C_1}$$

$$\omega_{z2} = \frac{1}{C_2\left(R_1 + R_3\right)}$$

Equation 2

Here ωp0, ωp2 and ωp3 are the compensator's poles and ωz1 and ω2 are its zeros. Of course Biricha Digital's automated power supply design software (Biricha WDS) automatically designs highly optimised compensators as discussed in the previous articles. However, if your transient response requirements are not very stringent, you can easily design a stable compensator by hand for most Buck/none-isolated Forward topologies.

Consider the Buck converter shown in Figure 1. We can see all the necessary values from this figure. Below is step-by-step on guidelines how to quickly design the compensator for this converter:

Step 1: Determine plant Bode plot

Setting the transformer turns ratio to 1:1 for now, for all Forward type topologies in voltage mode the plant bode plot is very simple; of course a Buck converter can be represented as a Forward converter with a transformer turns ratio of 1:1 .

Ignoring the PWM block for now, typically we have a resonant bump at 1/(2π √LC), and an ESR zero at 1/(2π ESR C). Using the values of L, C and ESR shown in figure 1,we can easily calculate the positions of the resonant bump and the ESR zero of the plant bode plot as shown on Figure 2.
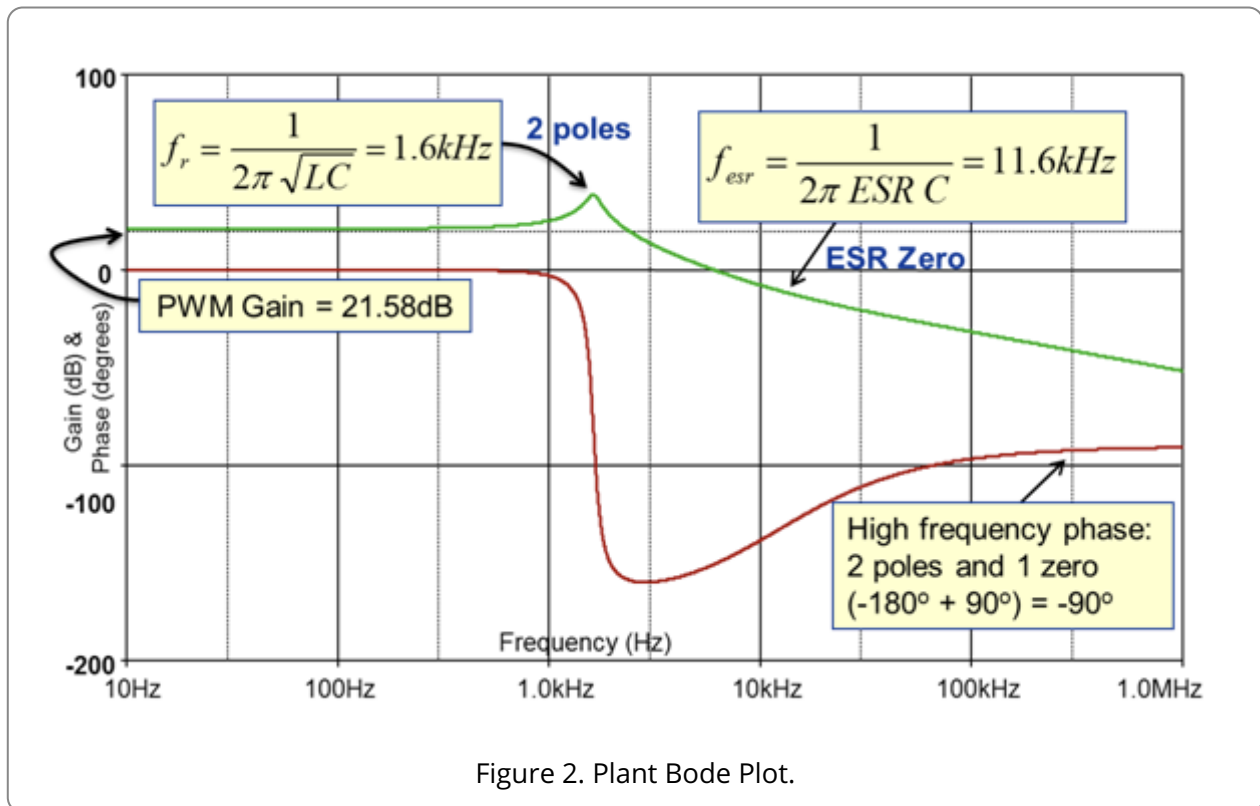

Figure 2. Plant Bode Plot.

From this figure, you will notice that unlike a standard LC filter, our low frequency gain is not 0dB. This is the impact of our PWM comparator and in many text books it is called the "PWM Gain". Again for voltage mode Buck converters this is very easy to calculate and is equal to our input voltage divided by the PWM ramp voltage of our controller IC, (i.e. Vramp in figure 1). We know our input voltage (12V in occur case) and the PWM ramp voltage is always specified in the datasheet of our IC (for simplicity we have taken this to be 1V). In our case therefore, the low frequency gain will be 20.Log(12V/1V) = 21.58dB.

Finally if we have a transformer in our circuit, all we need to do is to scale the gain plot by the transformer turns ratio. This completes the Bode plot of our plant and we can now design the compensator.

Step 2: Calculate Compensator pole/zero locations

The method presented here is an easy approximation to allow you to quickly calculate these for a compensator with relatively good performance with reasonable crossover frequencies. There are of course more accurate methods, and there are good books which have detailed analysis (please see the bibliography) but first and foremost, credit should be given to Dean Venable for his pioneering work in this field. Of course our WDS software uses exact equations to allows the user to specify exact phase margin and cross-over frequency; but for now all we need is a hand calculator and piece of paper.

You can see from the compensator's transfer function that we have 2 pole, 2 zeros and 1 pole at origin. To get reasonable performance:

1. Place 2 compensator zeros right on top of the plant's double poles (i.e. at 1.6kHz),
2. Place 1 compensator pole at ESR zero to cancel the plant's zero (i.e. at 11.6kHz),
3. Place the other compensator pole at half the switching frequency (i.e. if we have a switching frequency of 200kHz we place this pole at 100kHz). This will help in reducing high frequency noise,
4. Finally we place the pole at origin using Equation 3 below.

$$f_{p0} = \frac{V_{ramp} \times F_x}{V_{in}}$$

Equation 3

Where Fx is the desired cross-over frequency. In our case let us design for Fx = 10kHz and therefore we will have to place our pole at origin at 833 Hz (i.e. 1V×10kHz/12V).

Step 3: Calculate compensator component values

Now that we know the positions of our compensator poles and zeros, we can use the equations above to calculate component values in a step-by-step manner:

1.) I usually start by calculating R1 and Rb based on the current that I am willing to let through them and the reference voltage needed on my controller IC. I will then check to make sure that the power dissipation per resistor does not exceed ~60mW so that I don't get a hotspot on my PCB. I also try not to let the current fall below 100μA for robustness in the EMC test chamber during the susceptibility test.

R1 and Rb form a potential divider (or sampling divider) and this sets the demand reference voltage (in our case let us assume that this is 2.55V). So we know the input voltage of the potential divider (in our case this is Vout = 3.3V) and we know the output voltage of the potential divider fed to the IC (in our case 2.55V). Starting by allowing 1mA of current through this pot and using the standard potential divider equations and ohms law we have: R1 = 750□, Rb = 2.55kΩ, and power dissipation in each resistor < 60mW.

2 – Now that I know R1, I can use the equation for ωp0 to calculate C1 (please don't forget that these equation are all in rad/sec so we need to scale by 2π. Furthermore, C1 is usually much larger than C3 and therefore the equation for ωp0 simplifies to ωp0 = 1/ (R1×C1). I know R1, I know ωp0, so I can calculate C1(in our case C1 = 1 / (2π×833 Hz×750Ω) = 250nF.

3 –Equation for ωz1 is dependent on C1 and R2. We now know ωz1 and C1 so we can calculate R2 = 390π.

4 –Again as C1 >> C3 equation for ωp2 simplifies to ωp2 = 1/ (R2 C3). This pole is being placed on our ESR zero (i.e. @11.6kHz) and we know all the terms apart from C3 so we can calculate it. C3 = 34nF.

5 – Finally we are left with the equations for ωp3 and ωz2. These two are dependent on each other but we have 2 equations and 2 unknowns and therefore we can easily solve them. If we divide the equation for ωp3 by the equation for ωz2, then both C2 terms and the 2π terms cancel and we are

left with all the known variables and we can solve for R3:

$$\frac{\omega_{p3}}{\omega_{z2}} = \frac{(R_1 + R_3)}{R_3} \rightarrow \frac{100kHz}{1.6kHz} = \frac{750\Omega + R_3}{R_3}$$

Equation 4

With R3 calculated (in our case R3 = 12Ω) we can substitute back into equation for ωp3 and hence calculate our very last component: C2 = 130nF.

We can easily use WDS in "manual pole/zero placement" mode to verify our calculations. WDS provides us with all the important stability parameters as well the Bode plot. WDS Bode plot for our design is shown in figure 3 and the stability information is shown in Figure 4.
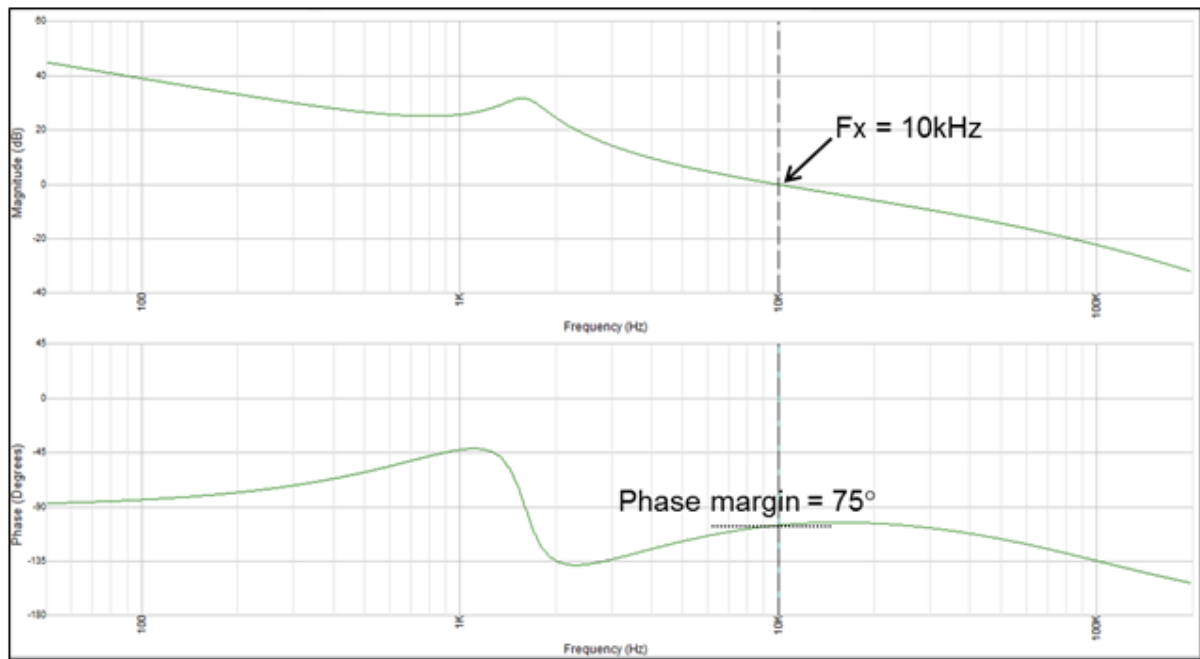

Figure 3. Simulated loop bode from Biricha WDS.

Figure 4. Stability data from WDS for our design.

From Figures 3 and 4, we can see that we have achieved a crossover frequency of 10kHz as desired and a phase margin of 75 degree. Slope at crossover is -20db/decade and our gain margin is better than 32dB. Thus we have design a very stable power supply with a respectable crossover frequency and even though we had no control over the phase margin, 75 degrees is more than ample.

Voltage Mode Compensator Design with Plants Containing a Transformer

If our Forward type topology has a transformer but no isolation (e.g. does not have an opto-coupler) then the design procedure is exactly the same as above with just one minor difference. All we have to do is to multiply our pole at origin by the turns ratio of our transformer.

For example if we had a Forward converter with exactly the same specification as the Buck converter in this article, but with a transformer turns ratio of 10:1 then all we would have to do is multiply our pole at origin by 10 (833 Hz × 10 = 8330Hz). The rest of the calculation and procedures will stay exactly the same.

Concluding Remarks

In this article, we discussed how to design a compensator for all hard switched Forward type non-isolated voltage mode converters. An approximate method has been presented that will give reasonable results in most cases. The advantage of the method presented here is that it is very easy and quick to calculate but we do not have any control over the phase margin. We also included a complete numerical example down to component value selection.

In the forthcoming articles we will discuss current mode control, isolation and why generally it is not a good idea to use a PID controller to stabilise a voltage mode power supply

Things to Try

1 – Download a copy of Biricha WDS PSU Design software (/wds)

2 – Attend one of our Analog Power Supply Design (/aps) workshops

2 – Visit OMICRON Lab website (http://www.omicron-lab.com/bode-100) for more information about Bode 100

Bibliography

[1] Biricha Digital's Analog Power Supply Design Workshop Manual

[2] Switching Power Supplies A – Z by Sanjay Maniktala, ISBN: 978-0123865335

[3] Switch-Mode Power Supplies, Second Edition: SPICE Simulations and Practical Designs by Christophe Basso, ISBN 978-0071823463