

ST WDS Installation Guide, User Guide and Design Example

Biricha Digital Power Ltd



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First, please download the latest version of ST WDS from www.biricha.com/st-wds

After downloading the WDS setup files, run the setup to being the installation. You may receive a warning from Windows - click "More Info" and "Run Anyway" to proceed.

When the installation beings you will be presented with the "Welcome" screen. Click "Next".



Please read the end-user license agreement (EULA) carefully. If you agree with the terms, select "I Agree" and click "Next" to continue. If you do not agree with the terms of the EULA then you should not proceed with the installation.

	HA AL WDS Installation Guide, User Guide and De	sign Example
///		
i.	'∰ wDs 🔶 🗖 🗖 🗖 🔂	
	License Agreement	
	Please take a moment to read the license agreement now. If you accept the terms below, click "I Agree", then "Next". Otherwise click "Cancel".	
	EULA	
	Please read this EULA carefully, as it sets out the terms and conditions upon which we license our Software for use.	
	By clicking "accept agreement" when you first install the Software, you agree to be bound by the terms and conditions of this EULA. You further agree that any person you authorise to use the Software will also be bound by the terms and conditions of this EULA. If you do not agree to this EULA you must click [*]	
	○ I Do Not Agree I Agree	
	Cancel < Back Next >	

Select the installation folder for WDS. The default installation folder is your "Program Files" directory. Click "Next" to continue.

🖞 WDS	• ×
Select Installation Folder	BIRICHA
The installer will install WDS to the following folder.	
To install in this folder, click "Next". To install to a different folder, enter it b	elow or click "Browse".
<u>F</u> older:	
C:\Program Files (x86)\Biricha Digital Power\WDS\	Browse
	Disk Cost
Install WDS for yourself, or for anyone who uses this computer:	
🔘 Everyone	
Just me	
Cancel < Back	Next >

Click "Next" to proceed with the installation.

JJ



You may receive a message about User Account Control from Windows, if so, click "Yes" to proceed with the installation.

i <mark>,</mark> ₩DS		
Installing WDS		BIRICHA DIGITAL
WDS is being installed.		
Please wait		
	Cancel	Back Next >

The installation is now complete. Click "Close" to exit the installer.



Setting up Licensing

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When downloading ST WDS you will have been presented with an activation code. Please copy this from your web browser to your clipboard. Then got to Help -> License and then paste your activation code into the relevant box. This will activate WDS.

If you do not have an activation code then WDS will run in trial mode. Under trial mode you have full access to all functions of WDS; the only limitation is that the input and output voltages are locked.

Updating WDS

In future, if your license file permits, WDS will prompt you when updates are available. Please ensure that you always update to the latest version.



Concept

- To begin, the user should select their preferred topology and enter an input voltage, output voltage and output current specification
- WDS will then calculate all other parameters based on this
- The user will then select parts from their supplier and then enter the actual values into WDS
- The design should start on the "Specification" tab and work through the tabs systematically. i.e. "Specification" to "Transformer" to "Semiconductor" to "Output Filter" to "Controller Design" etc.
- The ideal calculated values will automatically update as the users enters the actual values (such as selected transformer turns ratio, output capacitor, inductor, etc.)

Combo Boxes

- Combo boxes, such as the one shown below, are used to switch between WDS calculated values and user entered values
- WDS calculated values are shown with a blue background:



• If the user overwrites this with their own value, the background colour changes to white:



- WDS will use whatever value is currently active in the combo box. It is important to note that WDS will always use the user entered value over the WDS calculated value so if the user ever overwrites an calculated value, WDS will give priority to the user entered value.
- For your convenience, the nearest preferred values are calculated for many components and these can be selected by clicking the arrow to the right of the combo box
- The user can always switch back to the default WDS calculated value by clicking the arrow to the right of the combo box and selecting the value next to the text "(default)"



Calculated Values

• The locked text boxes on the left hand column indicated the original WDS calculated value and allow the user to compare the calculated value to the user defined value (if entered)



Design Example 1: Voltage Mode Buck Converter

Preamble

Within WDS you will be presented with a selection of tabs, edit boxes and combo boxes. There is a general design methodology is that you should start with the "Specification" tab and work your way across to the "Analog (Non-Isolated)" tab updating the relevant parameters with your design choice along the way.

The default calculated values are always highlighted in purple as shown in the picture below.

245.341 👻 🏴

You can edit this at any time by clicking into the box and overwriting them with your own value. The box will no longer be highlighted in purple indicating that your own value is being used. The value typed in by the user will always take precedence over the WDS calculated value. If at any time you wish to return to the default calculated value you can do so by clicking on the drop down arrow on the right hand side of the box and then selecting the option that says "(default)" next to it as shown in the screenshot below.



Specification Tab

On the "Specification" tab, enter the following specification into the relevant fields under "Converter Specification":

BIRICHA DIGITAL		WDS Instal	lation Guide, U	ser Guide	and Design Example
\checkmark	Converter Specification				
	Topology:	Buck		_	
	Output voltage isolated	d from primary side:	Non Isolated	T	
	Input Supply:				
	Maximum		12	V	

Output voltage isolated fi	rom primary side:	Non Isolated	-
Input Supply:			
Maximum		12	V
Nominal		12	V
Minimum		12	V
Output:			
Maximum Current		2	Α
Voltage		3.3	V
Output voltage ripple / over	shoot:		
Voltage Ripple (pk-pk)		0.5	%
Voltage Ripple (pk-pk)	16.5		mV
Load Step from 100% to		50	%
Voltage Overshoot	660	660 🗸	mV
Demand Efficiency	85	85 -	%

As you update the values, WDS will automatically update the design and show the associated Bode plot in the Frequency Response tab.

Again on the "Specification" tab, enter the following specification into the relevant fields under "Control Parameters":

Control Parameters			
Control Mode: Volta	age	•	
	Analog Control	Digital Control	
Switching Frequency		200	kHz
Sampling Frequency	n/a	n/a 👻	kHz
Pure Time Delay		n/a	x Tsamp
Crossover Frequency	20	10 👻	kHz
Phase Margin		55	Degrees

Note: The "Analog Control" option is not available within ST WDS. This feature is only available in the full version of WDS available form <u>www.biricha.com/wds</u>

Transformer Tab

Of course, the transformer tab is not applicable to the Buck converter. The boxes within this tab will be greyed out for all non-isolated topologies. However, for completeness we describe them here.

For an isolated power supply you would see a tab as shown below.

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Recommended (Np:1) gives the turns ratio of the transformer. The Primary Side Inductance of this transformer is calculated based on the user defined peak to peak ripple of the magnetizing current (Magnetizing Current Ripple (pk-pk) and the Secondary Side Inductance can then be calculated from the turns ratio. Finally recommended leakage is simply a set percentage of the Primary Side Inductance.

All worse case stresses are then calculate; e.g. Volts-Microseconds product. Note that Bias Winding Voltage is for documentation only and is not used.

Transformer					
Transformer Type	Center-Tapped	O Full-Wa	ave R	lectifier	
Recommended (Np:1)	1.124	1.124	\sim		
Magnetising Current Ripple	(pk-pk)	10		%	
Primary Side Inductance	134.919	134.919	~	μН	
Recommended Leakage	1.349	1.349	\sim	μН	
Volt-µSecond Product	31.725			V.µS	
Mag. Current (pk-pk)	200.121			mA	
Primary Current (pk)	2.168439			Α	
Primary RMS Current	1.155			Α	
Secondary RMS Current	1.239			А	
DCM/CCM Boundary	n/a			W	
Recommended values for c	alculations				
Pri. Winding Resistance	35.229	35.229	~	mΩ	
Sec. Winding Resistance	30.633	30.633	~	mΩ	
Copper Losses	0.094026			w	
PLB Remaining (core	0.093			w	
Bias Winding Voltage (if ap	plicable)	14		V	
Note: RMS/Average values are per					

Semiconductors Tab

Now move onto the "Semiconductors" tab, enter the following specification into the relevant fields under "Primary Switch"; these are the actual parameters of the FETs that we are using on the board. Important: for now, please ignore the values in the left hand column; these are calculated values based on your specification and will get updated as you input various parameters in the future tabs.

<	31.625	4.8	🛨 m!	Ω
<	25	25	🚽 ns	;
<	5	25	🚽 ns	;
<	1285.495	580	→ pF	-
	12.4		V	
nt	0.62		Α	
	1.118		Α	
	2.301		Α	
	0.006		W	
	0.147		W	
	< < < nt	< 31.625 < 25 < 5 < 1285.495 12.4 nt 0.62 1.118 2.301 0.006 0.147	 31.625 4.8 25 25 5 25 1285.495 580 12.4 0.62 1.118 2.301 0.006 0.147 	 31.625 4.8 mit 25 25 ns 25 25 ns 25 ns 25 ns 1285.495 580 pF 12.4 V 12.4 V 0.62 A 1.118 A 2.301 A 0.006 W 0.147

These are the values for the semiconductor switches that we are using on the Biricha Buck board used in our workshops.

Again on the "Semiconductors" tab, enter the following specification into the relevant fields under "Diode/Switch":

Diode/Switch					
Forward Voltage Drop	0.6	0.4	▼ V		
Peak Voltage Stress	11.989		v		
Average Current	1.38		Α		
RMS Current	1.667		Α		
Peak Current	2.301		Α		
Conduction Losses	0.552		w		
Recommended values for calculations					

Choke/Output Capacitor Tab

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Now click on the "Output Filter" tab. On the "Output Filter" tab, enter the following specification into the relevant fields under "Output Filter Inductor ":

Output Filter Inductor			
Specified Ripple (pk-pk)		25	▼ %
Specified Ripple (pk-pk)	0.5		Α
L0 Inductance	26.52	22	ΨH
L0 DCR		70	→ mΩ
Actual % Ripple (pk-pk)	30.1		%
Actual Ripple (pk-pk)	0.603		Α
Peak Current	2.301		Α
Average Current	2		Α
Power Dissipation	0.28		W
DCM/CCM Boundary	0.301022		Α
Recommended values for o	alculations		

Again this is the parameters of the Wurth inductor that we are using on the Biricha Buck board. Also on the "Output Filter" tab, enter the following specification into the relevant fields under "Output Filter Capacitor ":

Output Filter Capacitor					
C0 Capacitance	500.277	440 👻	μF		
C0 ESR	26.905	34 👻	mΩ		
C0 ESR Zero	10638.699		Hz		
Specified Overshoot	660		mV		
Actual Overshoot	49.643		mV		
Specified Ripple (pk-pk)	16.5		mV		
Actual Ripple (pk-pk)	20.107		mV		
RMS Current	0.17		Α		
Ripple Current (pk-pk)	0.591		Α		
Peak Voltage	3.32		V		
Power Dissipation	0.988		mW		
Recommended values for calculations					
Calculated capacitance is based on the voltage ripple requirement to meet both overshoot and voltage ripple specifications.					

Note that we are using 2x220uF caps and we measured the ESR to be around 70m Ω for 1 capacitor. So the ESR of 2 in parallel will be around 34.5m Ω .

Controller Design Tab

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On the "Controller Design" tab, WDS has selected a Type III compensator. The automatic pole/zero placement algorithms have calculated the location of the poles and zeros such that the loop will achieve the crossover frequency and phase margin specification concurrently, i.e. WDS has designed a compensator that will give a crossover of 10kHz and a phase margin of 55 degrees. As shown below:



Controller Poles and Zeros

Controller Poles and Zeros			
Automatic placement			
Pole at the origin	3979.289	3979.289 👻	Hz
First Pole	10638.699	10638.699 💌	Hz
Second Pole	100000	100000 -	Hz
First Zero	4860.243	4860.243 🔹	Hz
Second Zero	1601.229	1601.229 🔹	Hz

Note that in this tab WDS asks for the PWM ramp height which has been set to 1.8V

PWM Parameters		
PWM Ramp Height (pk-pk)	1.8	V

Note that this value is chip dependent. For the analog chip used in this example the typical value from the datasheet is 1.8V.

If not already in context, click on the "Frequency Response" tab on the right hand side to view the simulated Bode plot. Under the "Bode Plot" section of this tab, make sure that only "Loop" is ticked. This will display the simulated loop response. See that the simulated crossover frequency and phase margin are displayed at the top of this tab.

Analog (Non-Isolated)

Note: The "Analog (Non-Isolated)" option is not available within ST WDS. This feature is only available in the full version of WDS available form <u>www.biricha.com/wds</u>

Click on the "Analog (Non-Isolated)" tab. The component values required for the Type III compensator have been automatically calculated.

In this example we will be using an analog control IC to implement the controller.

The voltage reference from this chip is 5.1V. But, in this example, we divide this by 2 using a potential divider. Therefore in WDS please make sure that the "Error Amplifier Reference Voltage" is set to 2.55V.

Circuit Tab (right hand pane)

In WDS, click on the "Circuit" tab (right hand pane) and view the circuit diagram for the Type III compensator. Please study the circuit diagram and identify the location of the Type III compensator components.

Frequency Response (right hand pane)

Click on the "Frequency Response" tab (right hand pane) again to view the Bode plot. Then observe how the Bode plot changes as you type in the Nearest Preferred Values (NPVs) used in the actual circuit in to the relevant boxes in the "Controller Component Values" section of the "Analog (Non-Isolated)". The component values are shown below:



Controller Component Values			
R2	15.074	14	🚽 kΩ
R3	0.163	0.18	kΩ
C1	2.172	2.2	→ nF
C2	9.78	10	▼ nF
C3	1.827	1.5	▼ nF

WDS will always use the user defined values instead of calculated values. So now that you have changed the component values to their NPVs, your crossover and phase margin will also have changed. The simulated crossover frequency and phase margin have changed because you have now entered the values of the components used on the actual PCB, which are slightly different to those calculated by WDS. Thus your compensator poles and zeros are slightly different from the ones calculated by WDS.

Power Loss Budget Tab (right hand pane)

This tab toughly estimates the total power loss in various components of the power supply.

Total power loss budget (PLB) is estimated based on the user's efficiency requirements and this is displayed at the bottom light hand side of the WDS window. A warning is displayed of the losses exceed the total PLB.

Summary Tab (right hand pane)

This is the final summary of your design. It includes all the parameters calculated by WDS including all the voltage and current stresses on the devices in addition to all the frequency repose Bode plots.

When your design is complete, you can save this as an rft file by pressing the "Save Summary As" button or insert on your own reports by simply copying and pasting.

Finally pressing "Generate and Email Transformer Design to" allows you to generate an email with all the parameters relevant to the transformer which you can send to your magnetics supplier of choice.

Spice Simulation Tab (right hand pane)

This is an extremely power full feature full explanation of the available simulations is given when you click on this tab.



Design Example 2: Digital Voltage Mode Buck

Preamble

The design procedure is the same as Analog with the notable exception that instead of analog component values WDS will provide digital coefficients in various number formats.

Specification

On the "Specification" tab, enter the following specification into the relevant fields under "Converter Specification":

Converter Specification				
Topology: Bud	Topology: Buck			
Output voltage isolated from primary side: Non Isolated 👻				
Input Supply:				
Maximum		12	V	
Nominal		12	V	
Minimum		12	v	
Output:				
Maximum Current		2	Α	
Voltage		3.3	V	
Output voltage ripple / overs	hoot:			
Voltage Ripple (pk-pk)		0.5	%	
Voltage Ripple (pk-pk)	16.5		mV	
Load Step from 100% to		50	%	
Voltage Overshoot	660	660 -	mV	
Demand Efficiency	85	85 🗸	%	

Again on the "Specification" tab, enter the following specification into the relevant fields under "Control Parameters":

Control Parameters					
Control Mode: Voltage 💌					
	Analog Control	Oigital Control	bl		
Switching Frequency		350	kHz		
Sampling Frequency	350	350 👻	kHz		
Pure Time Delay		1	x Tsamp		
Crossover Frequency	17.5	15 👻	kHz		
Phase Margin		50	Degrees		

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As you update the values, WDS will automatically update the design and show the associated Bode plot in the Frequency Response tab.

Please note that I your sampling frequency is slower than your switching frequency WDS will automatically take this in to account and you do not need to add this in the Pure Time Delay box.

Semiconductors

Now move onto the "Semiconductors" tab, enter the following specification into the relevant fields under "Primary Switch"; these are the actual parameters of the FETs that we are using on the board. Important: for now, please ignore the values in the left hand column; these are calculated values based on your specification and will get updated as you input various parameters in the future tabs.

Primary Switch					
"On" Resistance	<	1	5 👻	mΩ	
Rise Time	<	5	10 👻	ns	
Fall Time	<	5	10 👻	ns	
Parasitic Cap (Coss)	<	10	490 🔻	рF	
Peak Switch Voltage		9.6		V	
Average Switch Curre	nt	0.638		Α	
RMS Switch Current		0.98		Α	
Peak Switch Current		1.652		Α	
Conduction Losses		0.005		W	
Switching Losses		0.06		W	
Recommended values for calculations					

These are the values for the semiconductor switches that we are using on the Biricha Buck board used in our workshops.

Again on the "Semiconductors" tab, enter the following specification into the relevant fields under "Diode/Switch":

Diode/Switch			
Forward Voltage Drop	0.6	0.6	▼ V
Peak Voltage Stress	8.991		V
Average Current	0.862		Α
RMS Current	1.143		Α
Peak Current	1.767		Α
Conduction Losses	0.517		W
Recommended values for ca	lculations		

Choke/Output Cap



Now click on the "Output Filter" tab. On the "Output Filter" tab, enter the following specification into the relevant fields under "Output Filter Inductor ":

Again this is the parameters of the Wurth inductor that we are using on the Biricha Buck board. Also on the "Output Filter" tab, enter the following specification into the relevant fields under "Output Filter Capacitor ":

Output Filter Inductor			
Specified Ripple (pk-pk)		25 👻	%
Specified Ripple (pk-pk)	0.375		Α
L0 Inductance	17.878	22 🔻	μH
L0 DCR		120 👻	mΩ
Actual % Ripple (pk-pk)	20.3		%
Actual Ripple (pk-pk)	0.305		Α
Peak Current	1.652		Α
Average Current	1.5		Α
Power Dissipation	0.27		W
DCM/CCM Boundary	0.152161		Α
Recommended values for c	alculations		

-0	utput Filter Capacitor			
	C0 Capacitance	148.733	440 ~	μF
	C0 ESR	44.375	34.5 🗸	mΩ
	C0 ESR Zero	10484.515		Hz
	Specified Overshoot	660		mV
	Actual Overshoot	42.092		mV
	Specified Ripple (pk-pk)	16.5		mV
	Actual Ripple (pk-pk)	12.21		mV
	RMS Current	0.102		Α
	Ripple Current (pk-pk)	0.354		Α
	Peak Voltage	3.312		V
	Power Dissipation	0.36		mW
	Recommended values for c	alculations		
	Calculated capacitance is b meet both overshoot and v stage filter).	ased on the volta voltage ripple spec	ge ripple requireme ifications (without	ent to second

Note that we are using 2x220uF caps and we measured the ESR to be around 70m Ω for 1 capacitor. The ESR of 2 in parallel will be around 34.5m Ω .



Controller Design

On the "Controller Design" tab, WDS has selected a Type III compensator. The automatic pole/zero placement algorithms have calculated the location of the poles and zeros such that the loop will achieve the crossover frequency and phase margin specification concurrently, i.e. WDS has designed a compensator that will give a crossover of 15kHz and a phase margin of 50 degrees (after phase erosion). As shown below:

Controller Poles and Zeros			
Automatic placement	nt 🔿 Man	ual placement	
Pole at the origin	2222.649	2222.649 V Hz	
First Pole	10484.515	10484.515 V Hz	
Second Pole	175000	175000 V Hz	
First Zero	2927.78	2927.78 V Hz	
Second Zero	1600.991	1600.991 V Hz	

If not already in context, click on the "Frequency Response" tab on the right hand side to view the simulated Bode plot. Under the "Bode Plot" section of this tab, make sure that only "Loop" is ticked. This will display the simulated loop response. See that the simulated crossover frequency and phase margin are displayed at the top of this tab.



Digital (Non-Isolated)



Click on the "Digital (Non-Isolated)" tab, enter the following into the relevant fields under "PWM Parameters"

PWM Parameters			
PWM Master Clock Frequer	псу	5440	MHz
Max PWM Period Count	15543	15543	~
MIN	0		
MAX	13988.7		

Again on the "Digital (Non-Isolated)" tab, enter the following into the relevant fields under "Sampling Divider and ADC":

Sampling Divider and ADC ADC Bits		12		bits
ADC Range		3.3		V
Pre-ADC Input Scaling	0.887	0.887	\sim	
Voltage on ADC Pin	2.927			V
REF	3632			

WDS will now be able to calculate the correct scaling factors for the digital controller.

Digital Controller Coefficients

WDS provides digital controller coefficients in floating point format suitable for the STM32 range of MCUs from STMicroelectronics. The general principle stays the same for all other coefficient formats.

Click on the "Coeffs (ST)" tab (on the right hand pane of WDS). WDS will then calculate the correct controller coefficients.

		Gutput Scaling Gain Factor	$\frac{B_3 Z^{-3} + B_2 Z^{-2} + B_1 Z^{-1} + B_0}{A_3 Z^{-3} - A_2 Z^{-2} - A_1 Z^{-1} + 1}$
B0 2.890319765773 A1 1.60594084667	B1 -2.660402717009	B2 -2.88612570593	B3 2.664596776852
	A2 -0.422105491844	A3 -0.183835354826	Copy to Clipboard

The user simply clicks "Copy to Clipboard" and then pastes the controller coefficients directly into their code.



Other Options

In this section we explain some other important options that may not have been covered with the above two examples

LTspice Simulations

WDS allows LTspice simulations in both time domain and frequency domain of your power supply, provided that LTspice is already installed. You can run a spice simulation by clicking in the "Spice Simulation" tab and then "Run LTspice Simulation" in the right hand window:

Frequency Response Circuit Power Lo	ss Dudget Summary Spice Simulation						
Options							
O Upen Loop	🔾 Yin Min	mum					
Closed Luop	● Vin Nut	ninel					
O Frequency Response (Warning	; takes several hours) () Vin Mur	imurn					
Path to L1 spice executable.	C\Program Files\) TCJ TspiceXVII(XVIb	84 exe					
Run I Topice Simulation							
WDS Spice Simulation							
parasitic elements within a typical conv	erter. This allows you to verify your design	and use the LTspice tools to mea	sure voltages and currents which may be	n interest to you.			
Open Loop Simulation							
(The open foop simulation has no feedba-	sk or controller. Instead, the switches are	driven with a fixed ('WW which is a	letermined based on the equations used i	WDS.			
Closed Lean Cimulation							
(The closed loop simulation implements t	he selected controller (both analog/digital	, isofated/non-isolated), This alfow	the user to test the feedback network for	tability			
and speed of response							
Frequency Response Simu	<u>llation</u>	in this out on The constants is si	nabilitati in charache chile and su canall sim	disciplicated into the			
feedback path of the power supply at a s	A unique memo or usang une requercy response or une convector is available using une opoint, me convector is sumatado to avaidy state and an strata signal is injected more the foedback path of the power supply of a specific frequency. The applicate signal is compared to the amplitude of the signal on the output of the convector (the convector).						
it has passed through the compensation function). The process is repeated for se	network and converter power stage). This woral frequencies in a logarithmic manner	provides the gain and phase of the and allows the full Bode plot to be	 control-to-output transfer function (also c obtained from a real time domain simulati 	alled open loop transfer in of the converter.			
No s-domain models are used. This freq	uency responce can then be overlayed on	top of the theoretical response by	ticking the "Spice" box on the Frequency	Response tab of WDS.			
to view the overlayed Bode plot	ials on a modern P.G. Alter bie fun simula	ton has infished (see the bottom o	the Erspice willowy please close Erspi	e and return to webs			
1							

Important: to import the results of your LTspice Simulation back into WDS you must close LTspice first.

For example if you run a "Frequency Response Simulation" in LTspice by activating it through WDS, after the simulation completed you must close LTspice. You can then click on the "Spice" button on the Bode plot to display the LTspice. In figure below green trace is WDS output and the black trace is the LTspice output imported in WDS.



Current Mode Converters

For Peak Current Mode, the options are almost exactly the same as voltage mode however in the "Controller Design" tab the user must enter the "Current Sense Gain" of the power supply. After that WDS will calculate how much compensating ramp is required and display in the "Amount of Ramp to Add" box. Please note that this is the height of ramp in volts if we were to allow the ramp to increase linearly for the entire Period T.

Isolated Power Supplies

You design an isolated power supply by simply selecting "Isolated" from the drop box in the Specification tab

Transformer

WDS provides most necessary information such as "turns ratio", "Volts-us" product etc. so that you or your magnetics design can design you're the magnetics WDS recommends the transformer turns ratio Primary inductance and leakage. The user can of course change these values after which all calculation will be based on the user's input. The user can also indicate if a bias winding is needed by filling in the "Bias Winding Voltage" box. Once all design parameters are completed in this tab the user can email this specification to his/her magnetics provider by pressing the "Generate and Email Transformer Design to" button on the "Summary" tab.

Output Capacitor Specification	Output Capacitor Controller Design Specification Transformer		Analog (Non-Isolated) Semiconductors					
Transformer								
Transformer Type	Transformer Type Center-Tapped			O Full-Wave Rectifier				
Recommended (Np	:1)	1.472	1.472	\sim				
Current Ripple (pk-pk)			80		%			
Primary Side Induc	Primary Side Inductance		25.336	\sim	μH			
Recommended Lea	Recommended Leakage		1.013	\sim	μH			
Coupling Capacitor	Coupling Capacitor		n/a	\sim	μF			
Volt-µSecond Product		35.25			V.µS			
Mag. Current (pk-pk)		n/a			mA			
Primary Current (pk)		1.903392			Α			
Primary RMS Current		0.986			Α			
Secondary RMS Current		1.452			Α			
DCM/CCM Boundary		2.99			W			
Recommended values for calculations								
Pri. Winding Resista	ance	18.257	18.257	~	mΩ			
Sec. Winding Resis	tance	8.426	8.426	~	mΩ			
Copper Losses		0.035511			w			
PLB Remaining (cor	e	-0.03			w			
loss) Bias Winding Voltage (if applicable)			14		v			
Note: RMS/Average values are per								

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